

ABSTRACT

According to one exemplary embodiment, a memory array comprises first and second isolation regions situated in a substrate, where the first and second isolation regions are separated by a separation distance. The memory array further comprises a trench situated between the first and second isolation regions, where the trench defines trench sidewalls and a trench bottom in the substrate. The memory array further comprises a tunnel oxide layer situated between the first and second isolation regions, where the tunnel oxide layer is situated on the trench sidewalls and the trench bottom. According to this embodiment, the memory array further comprises a channel region situated underneath the tunnel oxide layer and extending along the trench sidewalls and the trench bottom, where the channel region has an effective channel width, where the effective channel width increases as a height of the trench sidewalls increases.

**Figure 4B should accompany the Abstract.**